

A' ball connections are directly reflowed to the chip pads through vias formed in an intervening next level of substrate.

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Please replace the first paragraph on page 11 with the rewritten following paragraph:

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A2 Thus, as a key aspect of the present invention, substrate (150), preferably a bismaleimide triazine (BT), having a thickness between about 150 to 300 micrometers ( $\mu\text{m}$ ) is [mounted with] adhered to an adhesive layer (160), having a thickness between about 10 to 100  $\mu\text{m}$ . Layer (160) can be a polyimide thermocompression adhesive SPA made by Nippon Steel Chemical. The adhesive and the substrate together form an "adsubstrate" composite structure, reference numeral (165), as shown in Fig. 2c. The composite adsubstrate is then either mechanically drilled, or, preferably laser drilled with an area array of via openings (170) that correspond to AA I/O pads (110) or (140) on the chip, as shown in Fig. 2d. A top view of the adsubstrate with AA openings is also shown in Fig. 2e.

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Please replace the first paragraph on page 14 with the rewritten following paragraph:

A3 embodiment, is next prepared with drilled via openings (380) corresponding to the AA pad array on the CSPs to be attached as shown in Fig. 3c. It is preferred that substrate (370) comprises BT and has a thickness between about 150 to 300  $\mu\text{m}$ . Then the CSP of Fig. 3b is die attached to substrate (370), as shown in Fig. 3d. This is accomplished at a pressure between about 1.5 to 2.5 Mpascals and temperature between about 250 to 350  $^{\circ}\text{C}$ . The resulting package is next encapsulated (390) using a molding process as shown in Fig. 3e. This is followed by another key feature of the second embodiment, namely, a reflow ball mounting (400) process over openings (360) that connect to the AA I/O pads of the chip sites within the wafer, as shown in Fig. 3f. This is accomplished by forming solder comprising tin-lead or tin-silver alloy.

## IN THE CLAIMS

Please amend claims 1, 3, 11, 26 and claims 6, 16, 18 as follows:

A4 1. A Chip Scale Package (CSP) comprising: